

AMENDMENTS TO THE CLAIMS

Claim 1 (original): A method for writing to a memory element, said method comprising:
precharging a conductor to a first voltage value, said first voltage being held on said conductor by a capacitance associated with said conductor;
coupling a programmable conductor memory element between said first voltage on said conductor and a second voltage to write a predetermined resistance state in said memory element.

Claim 2 (original): A method as in claim 1 wherein said first voltage is higher than said second voltage to write a predetermined resistance state in said memory element.

Claim 3 (original): A method as in claim 1 wherein said first voltage is lower than said second voltage to write a predetermined resistance state in said memory element,

Claim 4 (original): A method as in claim 1 wherein said associated capacitance comprises a parasitic capacitance of said conductor.

Claim 5 (original): A method as in claim 1 wherein said associated capacitance comprises a capacitor coupled to said conductor.

Claim 6 (original): A method as in claim 1 wherein said associated capacitance comprises a parasitic capacitance of said conductor and a capacitor coupled to said conductor.

Claim 7 (original): A method as in claim 1 wherein said programmable conductor memory element is coupled to said conductor by enabling an access transistor.

Claim 8 (original): A method as in claim 2 wherein said first voltage is at or approximately at V_{dd} and said second voltage is $V_{dd}/2$.

Claim 9 (previously presented): A method as in claim 3 wherein said first voltage is ground and said second voltage is at or approximately at $V_{dd}/2$.

Claim 10 (original): A method as in claim 1 wherein said conductor is a bit line associated with said memory element.

Claim 11 (original): A method as in claim 1 wherein said memory element comprises a chalcogenide glass memory element.

Claim 12 (original): A method as in claim 11 wherein said chalcogenide glass memory element comprises a germanium:selenium glass composition which is doped with silver.

Claim 13 (original): A method for writing a semiconductor memory cell, the method comprising:

applying a first predetermined voltage to a first terminal of a programmable conductor memory element;

charging a bit line of a memory array to which said memory cell belongs to a second predetermined voltage, said bit line having a parasitic capacitance which stores said second predetermined voltage;

applying a third predetermined voltage to a gate of a transistor to enable said transistor and couple said bit line to a second terminal of said programmable conductor memory element;
and

using a voltage across said memory element when said transistor is enabled to establish a resistance state of said memory element.

Claim 14 (original): The method of claim 13 wherein said second predetermined voltage is greater than said first predetermined voltage.

Claim 15 (original): The method of claim 13 wherein said first predetermined voltage is greater than said second predetermined voltage.

Claim 16 (original): The method of claim 13 wherein said voltage across said memory element is discharged through said memory element to establish said resistance state.

Claim 17 (original): The method of claim 13 wherein said first predetermined voltage is at or approximately at $V_{dd}/2$ and said second predetermined voltage is at or approximately at V_{dd} .

Claim 18 (original): The method of claim 13 wherein said first predetermined voltage is at or approximately at $V_{dd}/2$ and said second predetermined voltage is at or approximately at ground.

Claim 19 (original): The method of claim 13 wherein said act of applying a first predetermined voltage comprises coupling a cell plate, to which said first terminal is coupled, to a source of said first predetermined voltage.

Claim 20 (original): The method of claim 13 further comprising the step of selectively coupling at least one capacitor to said bit line to store said second predetermined voltage.

Claim 21 (original): The method of claim 20 further comprising enabling a transistor to selectively couple at least one capacitor to said bit line.

Claim 22 (original): The method of claim 13 wherein said parasitic capacitance has a value of about 500 fF.

Claim 23 (original): The method of claim 13 wherein said programmable conductor memory element comprises a chalcogenide glass.

Claim 24 (original): The method of claim 23 wherein said chalcogenide glass comprises a Ge:Se glass composition which is doped with silver.

Claim 25 (original): A method of operating a memory cell, said method comprising:
precharging a bit line to a first voltage;
applying a second voltage to a first terminal of a chalcogenide memory element; and
connecting a second terminal of said chalcogenide memory element to said bit line to produce a voltage across said memory element sufficient to write a predetermined resistance state into said memory element.

Claim 26 (original): The method of claim 25 wherein said second voltage is greater than said first voltage.

Claim 27 (original): The method of claim 25 wherein said first voltage is greater than said second voltage.

Claim 28 (original): The method of claim 25 wherein said first voltage is held on said bit line by a parasitic capacitance.

Claim 29 (original): The method of claim 25 further comprising selectively coupling at least one capacitor to said bit line to receive and store said first voltage.

Claim 30 (original): The method of claim 29 further comprising operating a transistor to selectively couple said at least one capacitor to said bit line.

Claim 31 (original): The method of claim 25 wherein said bit line has a parasitic capacitance of about 500 fF.

Claim 32 (original): The method of claim 25 wherein said chalcogenide memory element comprises a Ge:Se glass composition doped with silver.

Claim 33 (original): The method of claim 25 wherein said connecting further comprises enabling a transistor to connect said second terminal to said bit line.

Claim 34 (original): The method of claim 33 wherein said transistor is enabled by a word line voltage applied to a gate of said transistor.

Claim 35 (original): A memory structure comprising:

a conductor having an associated capacitance;

a precharge circuit for precharging said conductor to a first voltage, said first voltage being held on said conductor by said associated capacitance;

a programmable conductor memory element having one terminal connected to a second voltage; and

an access device for selectively coupling a second terminal of said memory element to said conductor, said access device enabling said first and second voltages to establish a voltage across said programmable element sufficient to program said memory element to one of a higher and lower resistance state.

Claim 36 (original): The memory structure of claim 35 wherein said access device is a transistor.

Claim 37 (original): The memory structure of claim 35 wherein said precharge circuit supplies a first value as said first voltage to program a higher resistance state into said

memory element and a second value as said first voltage to program a lower resistance state into said memory element.

Claim 38 (original): The memory structure of claim 37 wherein said first value is at or approximately at Vdd, said second value is ground, and said second voltage is at or approximately at Vdd/2.

Claim 39 (original): The memory structure of claim 35 wherein said associated capacitance comprises a parasitic capacitance of said conductor.

Claim 40 (original): The memory structure of claim 35 wherein said associated capacitance comprises at least one capacitor coupled to said conductor.

Claim 41 (original): The memory structure of claim 35 wherein said associated capacitance comprises a parasitic capacitance of said conductor and at least one capacitor coupled to said conductor.

Claim 42 (original): The memory structure of claim 35 wherein said conductor is a bit line and said access device is enabled by a voltage applied to a word line.

Claim 43 (original): The memory structure of claim 35 wherein said memory element comprises a chalcogenide glass memory element.

Claim 44 (original): The memory structure of claim 43 wherein said chalcogenide glass memory element comprises a Ge:Se glass composition which is doped with silver.

Claim 45 (original): A semiconductor memory comprising:
a bit line having an associated capacitance;

a programmable conductor memory element having first and second terminals;
a precharge circuit for precharging said bit line to one of two possible voltage values depending on a desired state of resistance programming of said memory element, said associated capacitance holding a precharge voltage value on said bit line;
a cell plate coupled to a first terminal of said memory element for supplying a third voltage value to said first terminal; and
an access transistor responsive to a voltage on a word line for selectively coupling said bit line to said second terminal of said memory element to program said memory element to a resistance state based on the voltage values on said cell plate and bit line.

Claim 46 (original): The semiconductor memory of claim 45 wherein one of said two possible voltage values is higher than said third voltage value and the other of said two possible voltage values is lower than said third voltage value.

Claim 47 (original): The semiconductor memory of claim 45 wherein said associated capacitance comprises a parasitic capacitance of said conductor.

Claim 48 (original): The semiconductor memory of claim 45 wherein said associated capacitance comprises at least one capacitor coupled to said conductor.

Claim 49 (original): The semiconductor memory of claim 45 wherein said associated capacitance comprises a parasitic capacitance of said conductor and at least one capacitor coupled to said conductor.

Claim 50 (original): The semiconductor memory of claim 48 further comprising a switching device for selectively coupling said at least one capacitor to said bit line.

Claim 51 (original): The semiconductor memory of claim 49 comprising a switching device for selectively coupling said at least one capacitor to said bit line.

Claim 52 (original): The semiconductor memory of claim 45 wherein said memory element comprises a chalcogenide glass memory element.

Claim 53 (original): The semiconductor memory of claim 52 wherein said chalcogenide glass memory element comprises a Ge:Se glass composition which is doped with silver.

Claim 54 (original): The memory of claim 47 wherein said parasitic capacitance has a value of about 500 fF.

Claim 55 (currently amended): A memory cell comprising:
a chalcogenide memory element having first and second terminals;
a first memory line;
a circuit for selectively precharging said first memory line to either a first or second voltage;
a circuit for supplying a third voltage to the first terminal of said chalcogenide element; and
a device for switchably coupling the second terminal of said chalcogenide memory element to said first memory line after said first memory line has been precharged, said device causing a voltage to be applied across said chalcogenide memory element sufficient to write one of two predetermined resistance states in said chalcogenide element depending on which of said first or second voltage is precharged on said memory line.

Claim 56 (original): The memory cell of claim 55 wherein said third voltage is between said first and second voltages.

Claim 57 (original): The memory cell of claim 55 wherein said memory line further comprises a parasitic capacitance for holding an applied precharge voltage.

Claim 58 (original): The memory cell of claim 55 further comprising at least one capacitor coupled to said memory line to receive and hold said precharge voltage.

Claim 59 (original): The memory cell of claim 58 further comprising a switching device for selectively coupling said at least one capacitor to said memory line.

Claim 60 (original): The memory of claim 57 wherein said memory line has a parasitic capacitance of about 500 fF.

Claim 61 (original): The memory of claim 55 wherein said chalcogenide memory element comprises a germanium:selenium glass composition which is doped with silver.

Claim 62 (original): A processor system comprising:

a processor; and

a semiconductor memory coupled to said processor, said semiconductor memory comprising:

a conductor having an associated capacitance;

a precharge circuit for precharging said conductor to a first voltage, said first voltage being held on said conductor by said associated capacitance;

a programmable conductor memory element having one terminal connected to a second voltage; and

an access device for selectively coupling a second terminal of said memory element to said conductor, said access device enabling said first and second voltages to establish a voltage across said programmable element sufficient to program said memory element to one of a higher and lower resistance state.

Claim 63 (original): The processor system of claim 62 wherein aid access device is a transistor.

Claim 64 (original): The processor system of claim 62 wherein said precharge circuit supplies a first value as said first voltage to program a higher resistance state into said memory element and a second value as said first voltage to program a lower resistance state into said memory element.

Claim 65 (original): The processor system of claim 64 wherein said first value is at or approximately at Vdd, said second value is at or approximately at ground, and said second voltage is at or approximately at Vdd/2.

Claim 66 (original): The processor system of claim 62 wherein said associated capacitance comprises a parasitic capacitance of said conductor.

Claim 67 (original): The processor system of claim 62 wherein said associated capacitance comprises at least one capacitor coupled to said conductor.

Claim 68 (original): The processor system of claim 62 wherein said associated capacitance comprises a parasitic capacitance of said conductor and at least one capacitor coupled to said conductor.

Claim 69 (original): The processor system of claim 62 wherein said conductor is a bit line and said access device is enabled by a voltage applied to a word line.

Claim 70 (original): The processor system of claim 62 wherein said memory element comprises a chalcogenide glass memory element.

Claim 71 (original): The processor system of claim 70 wherein said chalcogenide glass memory element comprises a Ge:Se glass composition which is doped with silver.